



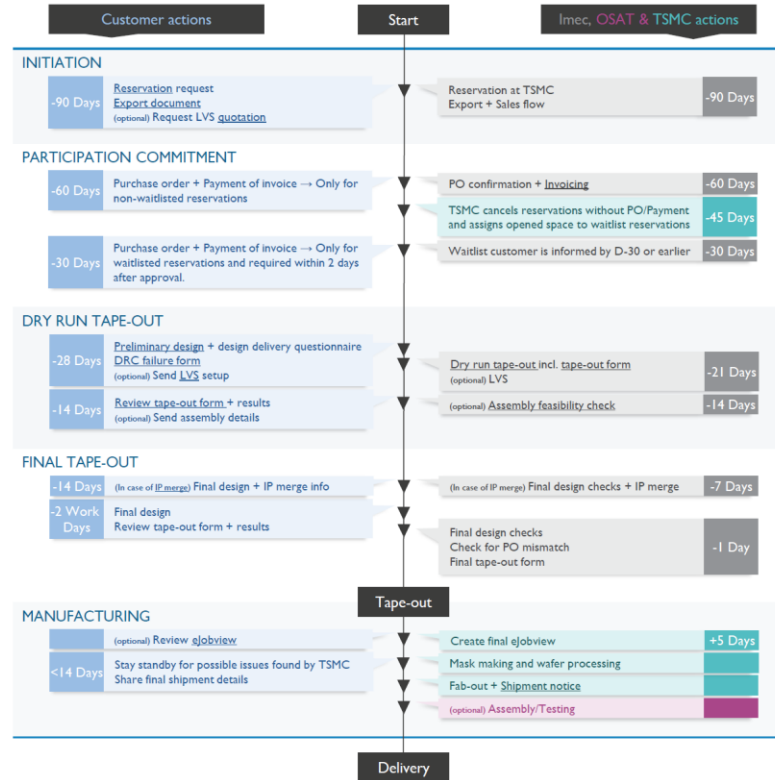
TSMC CyberShuttle Schedule 2027

October 2026 – v 1.0

CyberShuttle Reservations for 2027 Shuttles

					
Early October	M - 3 months	D - 60 days	D - 45 days	D - 30 days	D-day
✓ Release of entire year's schedule for ≥N12 ✓ Release half-year schedule for ≤N7, second half on March 17	✓ Select your CyberShuttle <u>before this date</u> and make a reservation through this reservation form.	✓ Cutoff date purchase order and EUQ.	✓ Seats without payment will be canceled. ✓ Free vacancies will be offered to wait-listed customers. ✓ imec/TSMC will approve and inform waitlisted customers.	✓ MPW acceptance cutoff date for waitlisted designs	✓ Tape-in date and launch of the CyberShuttle

CyberShuttle project timeline



Schedules 2027

1.4nm ~ 7nm

Technology	Flavor	Month	Shuttle ref	Fab	Reserve before	Purchase order before	Dry run GDS	Final GDS*	Tape-out	Estimated shipment date
1.4nm	Logic, Nanosheet Plus (0.75V)	May	TM0C96	20	Jan 27	Mar 2	Apr 3	Apr 29 TBC	May 1 TBC	Oct 9- Nov 13
2nm	Logic, Nanosheet Plus (0.75V, shrink)	January	TM0C86	22	Oct 5 2026	Nov 6 2026	Dec 2	Jan 3	Jan 5	Jun 15-Jul 20
		April	TM0C87	22	Dec 28 2026	Feb 12	Mar 17	Apr 11	Apr 13	Sep 21-Oct 26
		The 2nm Cybershuttle deadline(s) for the second half of 2027 will be known in March '27								
3nm	Logic, FinFET (0.75/1.2V, shrink) Logic, FinFET Compact (0.75/1.2V, shrink)	March	TM0C90	18	Nov 25 2026	Jan 15	Feb 17	Mar 14	Mar 16	Aug 11-Sep 15
		June	TM0C91	18	Mar 1	Apr 23	May 26	Jun 20	Jun 22	Nov17-Dec 22
		The 3nm Cybershuttle deadline(s) for the second half of 2027 will be known in March '27								
4nm	Logic, FinFET Plus (0.75/1.2V) Logic, FinFET Compact (0.75/1.2V)	May	TM0C68	18	Jan 27	Mar 12	Apr 14	May 09	May 11	Sep 17-Oct 22
		The 4nm Cybershuttle deadline(s) for the second half of 2027 will be known in March '27								
5nm	Logic FinFET (FF) (0.75/1.2V)	June	TM0C70	18	Feb 28	Apr 16	May 19	Jun 13	Jun 15	Oct 28-Dec 02
		The 5nm Cybershuttle deadline(s) for the second half of 2027 will be known in March '27								
6nm	Logic FinFET (0.75/1.8V)	February	TM0C75	15	Oct 26 2026	Dec 22 2026				
		The 6nm Cybershuttle deadline(s) for the second half of 2027 will be known in March '27								
7nm	Logic FinFET (0.75/1.8V)	January	TM0C77	15	Oct 5 2026	Nov 20	Dec 23 2026	Jan 17	Jan 19	May 17-Jun 21
		The 7nm Cybershuttle deadline(s) for the second half of 2027 will be known in March '27								

* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.

12nm ~ 16nm

Technology	Flavor	Month	Shuttle ref	Fab	Reserve before	Purchase order before	Dry run GDS	Final GDS*	Tape-out	Estimated shipment date
12nm	Logic FinFET Compact (0.8/1.8V) Logic FinFET Compact Plus (0.8/1.8V) RF FinFET Compact Plus (0.8/1.8V)	February	TM0C80	14	Oct 26 2026	Dec 22 2026	Jan 25	Feb 19 12PM	Feb 22	May 22-Jun 26
		April	TM0C81	14	Dec 28 2026	Feb 25	Mar 29	Apr 23 12PM	Apr 26	Jul 24-Aug 28
		June	TM0C82	14	Mar 1	Apr 29	May 31	Jun 25 12PM	Jun 28	Sep 27-Oct 30
		August	TM0C83	14	Apr 28	Jul 1	Aug 2	Aug 27 12PM	Aug 30	Nov 27- Jan 02 2028
		October	TM0C84	14	Jun 25	Aug 19	Sep 20	Oct 15 12PM	Oct 18	Jan 15-Feb 19 2028
16nm	Logic FinFET Compact (0.8/1.8V) Logic FinFET Compact Plus (0.8/1.8V) Logic FinFET Plus (0.8/1.8V) RF FinFET Compact (0.8/1.8V) ***	February	TM0C80	14	Oct 26 2026	Dec 22 2026	Jan 25	Feb 19 12PM	Feb 22	May 22-Jun 26
		April	TM0C81	14	Dec 28 2026	Feb 25	Mar 29	Apr 23 12PM	Apr 26	Jul 24-Aug 28
		June	TM0C82	14	Mar 1	Apr 29	May 31	Jun 25 12PM	Jun 28	Sep 27-Oct 30
		August	TM0C83	14	Apr 28	Jul 1	Aug 2	Aug 27 12PM	Aug 30	Nov 27- Jan 02 2028
		October	TM0C84	14	Jun 25	Aug 19	Sep 20	Oct 15 12PM	Oct 18	Jan 15-Feb 19 2028
		December	TM0C85	14	Aug 25	Oct 14	Nov 15	Dec 10 12PM	Dec 13	Mar 11-Apr 15 2028

* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.
For FinFet designs, meeting the 12 PM CET cutoff is essential to ensure sufficient time for validation and feedback before the tape-out.

22nm ~ 28nm

Technology	Flavor	Month	Shuttle ref	Fab	Reserve before	Purchase order before	Dry run GDS	Final GDS*	Tape-out	Estimated shipment date
22nm	Logic ULL (0.8/1.8V, 0.8/2.5V) Logic ULP (0.8/1.8V, 0.8/2.5V) MRAM RF ULL (0.8/1.8V, 0.8/2.5V) MRAM ULL (0.8/1.8V, 0.8/2.5V) ReRAM RF ULL (0.8/2.5V) RF ULL (0.8/1.8V, 0.8/2.5V) RF ULP (0.8/1.8V)	January	TM0CA0	15	Oct 05 2026	Nov 13 2026	Dec 16 2026	Jan 10	Jan 12	Apr 07-May 12
		March	TM0CA1	15	Nov 25 2026	Jan 15	Feb 17	Mar 14	Mar 16	Jun 09-Jul 14
		April	TM0CA2	15	Dec 28 2026	Feb 12	Mar 17	Apr 11	Apr 13	Jul 07-Aug 11
		May	TM0CA3	15	Jan 27	Mar 12	Apr 14	May 9	May 11	Aug 04-Sep 08
		July	TM0CA4	15	Mar 25	May 14	Jun 16	Jul 11	Jul 13	Oct 06-Nov 10
		August	TM0CA5	15	Apr 28	Jun 25	Jul 28	Aug 22	Aug 24	Nov 17-Dec 22
		September	TM0CA6	15	May 25	Jul 23	Aug 25	Sep 19	Sep 21	Dec 15-Jan 19 2028
		November	TM0CA7	15	Jul 27	Sep 17	Oct 20	Nov 14	Nov 16	Feb 09-Mar 15 2028
		December	TM0CA8	15	Aug 25	Oct 21	Nov 21	Dec 16	Dec 20	Mar 14-Apr 18 2028
28nm	Logic, HP (0.85/1.8V, 0.85/2.5V) Logic, HPL (1.0&1.8V, 1.0/2.5V) Logic, HPC (0.9/1.8V, 0.9/2.5V) Logic, HPC Plus (0.9/1.8V, 0.9/2.5V) Logic, HPM (0.9/1.8V, 0.9/2.5V) Logic, LP (1.05/1.8V, 1.05/2.5V) RF HPL (1.0/1.8V, 1.0/2.5V) RF HPC (0.9/1.8V, 0.9/2.5V) RF HPC Plus (0.9/1.8V, 0.9/2.5V) RF LP (1.05V/1.8V)	January	TM0CB0	15	Oct 05 2026	Nov 13 (2026)	Dec 16 2026	Jan 10	Jan 12	Apr 01-May 06
		February	TM0CB1	15	Oct 26 2026	Dec 22 (2026)	Jan 27	Feb 21	Feb 23	May 13-Jun 17
		March	TM0CB2	15	Nov 25 2026	Jan 22	Feb 24	Mar 21	Mar 23	Jun 10-Jul 15
		May	TM0CB3	15	Jan 27	Mar 19	Apr 21	May 16	May 18	Aug 05- Sep 09
		June	TM0CB4	15	Mar 1	Apr 16	May 19	Jun 13	Jun 15	Sep 02-Oct 07
		August	TM0CB5	15	Apr 28	Jun 18	Jul 21	Aug 15	Aug 17	Nov 04-Dec 09
		September	TM0CB6	15	May 25	Jul 23	Aug 25	Sep 19	Sep 21	Dec 09-Jan 13 2028
		November	TM0CB7	15	Jul 27	Sep 17	Oct 20	Nov 14	Nov 16	Feb 03-Mar 09 2028
		December	TM0CB8	15	Aug 25	Oct 15	Nov 17	Dec 12	Dec 14	Mar 02-Apr 06 2028

* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to epsmc@imec.be at the purchase order stage.

40nm

Technology	Flavor	Month	Shuttle ref	Fab	Reserve before	Purchase order before	Dry run GDS	Final GDS*	Tape-out	Estimated shipment date
40nm	EmbFlash 40LP (1.1/2.5V) ** EmbFlash 40ULP (0.9V/2.5V) **	February	TM0CC1	14	Oct 26 2026	Dec22 2026	Jan 25	Feb 18	Feb 22	May 31-Jul 05
		June	TM0CC3	14	Mar 1	Apr 22	May 24	Jun 17	Jun 21	Sep 27-Nov 01
		August	TM0CC4	14	Apr 28	Jun 17	Jul 19	Aug 12	Aug 16	Nov 22-Dec27
		December	TM0CC6	14	Aug 25	Oct 21	Nov 22	Dec 16	Dec 20	Mar 27-May 01 2028
	High Voltage (1.1/5/6/25/32V) High Voltage (1.1/8/25V)	April	TM0CC2	12	Dec 28 2026	Feb 18	Mar 22	Apr 15	Apr 19	Jul 16- Aug 20
		October	TM0CC5	12	Jun 25	Aug 19	Sep 20	Oct 14	Oct 18	Jan 14- Feb 18 2028
	Logic 40LP (1.1/1.8V, 1.1/2.5V) Logic 40ULP (1.1/2.5V, 0.9/2.5V) Mixed-Signal/RF 40LP (1.1/1.8V, 1.1/2.5V) Mixed-Signal/RF 40ULP (1.1/2.5V, 0.9/1.8V, 0.9/2.5V)	February	TM0CC1	14	Oct 26 2026	Dec22 2026	Jan 25	Feb 18	Feb 22	May 05-Jun 09
		April	TM0CC2	12	Dec 28 2026	Feb 18	Mar 22	Apr 15	Apr 19	Jun 30-Aug 04
		June	TM0CC3	14	Mar 1	Apr 22	May 24	Jun 17	Jun 21	Sep 01-Oct 06
		August	TM0CC4	14	Apr 28	Jun 17	Jul 19	Aug 12	Aug 16	Oct 27-Dec 01
		October	TM0CC5	12	Jun 25	Aug 19	Sep 20	Oct 14	Oct 18	Dec 29-Feb 02 2028
		December	TM0CC6	14	Aug 25	Oct 21	Nov 22	Dec 16	Dec 20	Mar 01-Apr 05 2028
	Logic 45GS (45GS = 40G) (0.9/1.8V, 0.9/2.5V)	April	TM0CC2	12	Dec 28 2026	Feb 18	Mar 22	Apr 15	Apr 19	Jun 30-Aug 04
		October	TM0CC5	12	Jun 25	Aug 19	Sep 20	Oct 14	Oct 18	Dec 29-Feb 02 2028
	ReRAM RF 40ULP (0.9V/2.5V)	April	TM0CC2	12	Dec 28 2026	Feb 18	Mar 22	Apr 15	Apr 19	Jul 13-Aug 17
		October	TM0CC5	12	Jun 25	Aug 19	Sep 20	Oct 14	Oct 18	Jan 11-Feb 15 2028

* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to epetsmc@imec.be at the purchase order stage. Meeting the 12 PM CET cutoff is essential to ensure sufficient time for validation and feedback before the tape out

55nm ~ 65nm

Technology	Flavor	Month	Shuttle ref	Fab	Reserve before	Purchase order before	Dry run GDS	Final GDS*	Tape-out	Estimated shipment date
55nm	Logic GP (1.0/1.8V, 1.0/2.5V), LP (1.2/2.5V), ULP (0.9V/2.5V) Mixed Signal/RF ULP (0.9V/2.5V), LP (1.2/ 2.5V)	May	TM0CA9	14	Jan 27	Mar 19	Apr 21	May 16	May 18	Jul 26-Aug 30
	EmbFlash (1.2/2.5V), ULP (0.9&2.5V) **	May	TM0CA9	14	Jan 27	Mar 19	Apr 21	May 16	May 18	Aug 08-Sep 12
65nm**	Logic GP /DGO (1.0/1.8V, 1.0/2.5V, 1.0/3.3V) Logic LP/DGO (1.2/2.5V, 1.2/3.3V) Logic ULP (1.0/2.5V) Mixed-Signal/RF GP(1.0/ 2.5V) Mixed-Signal/RF LP(1.2/ 2.5V)	January	TM0CD1	14	Oct 05	Nov 06	Dec 02	Dec 22 2026	Jan 05	Mar 16-Apr 20
		March	TM0CD2	12	Nov 25	Jan 02	Feb 03	Feb 28	Mar 02	May 11-Jun 15
		April	TM0CD3	14	Dec 28 2026	Feb 19	Mar 24	Apr 18	Apr 20	Jun 29-Aug 03
		June	TM0CD4	14	Mar 01	Apr 23	May 26	Jun 20	Jun 22	Aug 31-Oct 05
		July	TM0CD5	12	Mar 25	May 14	Jun 16	Jul 11	Jul 13	Sep 21-Oct 26
		September	TM0CD6	14	May 25	Jul 09	Aug 11	Sep 05	Sep 07	Nov 16-Dec 21
		November	TM0CD7	12	Jul 27	Sep 3	Oct 6	Oct 31	Nov 2	Jan 11-Feb 15 2028
		December	TM0CD8	14	Aug 27	Oct 1	Nov 3	Nov 28	Nov 30	Feb 08-Mar 14 2028
	Logic LP-based TGO (1.0/1.2/2.5V)	March	TM0CD2	12	Nov 25 2026	Jan 02	Feb 3	Feb 28	Mar 2	May 11-Jun 15
		July	TM0CD5	12	Mar 25	May 14	Jun 16	Jul 11	Jul 13	Sep 21-Oct 26
		November	TM0CD7	12	Jul 27	Sep 3	Oct 6	Oct 31	Nov 2	Jan 11-Feb 15 2028

* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.

** 65nm eFuse is only supported in FabI2. Please select the correct CyberShuttle.

0.18um Logic/Mixed-Signal/RF G (1.8/3.3V) + EmbFlash/OTP/MTP

Technology	Flavor	Month	Shuttle Ref	Fab	Reserve before	Purchase order before	Dry run GDS	Final GDS*	Tape-out	Estimated shipment date
0.18um	Logic, G (1.8/3.3V) Mixed-signal/RF, G (1.8/3.3V)	January	TM0CE1	8	Oct 05 2026	Nov 20 2026	Dec 23 2026	Jan 17	Jan 19	Mar 09-Apr 13
		March	TM0CE2	SSMC**	Nov 25 2026	Jan 08	Feb 10	Mar 07	Mar 09	May 11-Jun 15
		April	TM0CE3	6	Dec 28 2026	Feb 26	Mar 31	Apr 25	Apr 27	Jun 11-Jul 16
		July	TM0CE6	3	Mar 25	May 14	Jun 16	Jul 11	Jul 13	Aug 27-Oct 01
		July	TM0CE7	8	Mar 25	May 21	Jun 23	Jul 18	Jul 20	Sep 07-Oct 12
		August	TM0CE8	6	Apr 28	Jun 25	Jul 28	Aug 21	Aug 24	Oct 08-Nov 12
		September	TM0CE9	SSMC**	May 25	Jul 9	Aug 11	Sep 5	Sep 7	Nov 09-Dec14
		October	TM0CF1	6	Jun 25	Aug 27	Sep 29	Oct 24	Oct 26	Dec 10-Jan 14 2028
		November	TM0CF3	8	Jul 27	Sep 10	Oct 13	Nov 7	Nov 9	Dec 29-Feb 01 2028
		November	TM0CF2	3	Jul 27	Sep 24	Oct 27	Nov 21	Nov 23	Jan 07-Feb 11 2028
	EmbFlash Enhanced (1.8/3.3V & 1.8/5V)	November	TM0CF2	3	Jul 27	Sep 24	Oct 27	Nov 21	Nov 23	Feb 01-Mar 07 2028
0.18um	Logic, G (1.8/3.3V) Embedded OTP/MTP Mixed-signal/RF, G (1.8/3.3V) embedded MTP Mixed-signal/RF, G (1.8/3.3V) OTP Kilopass/eMemory	January	TM0CE1	8	Oct 05 2026	Nov 20 2026	Dec 23 2026	Jan 17	Jan 19	Mar 09-Apr 13
		April	TM0CE3	6	Dec 28 2026	Feb 26	Mar 31	Apr 25	Apr 27	Jun 11-Jul 16
		July	TM0CE6	3	Mar 25	May 14	Jun 16	Jul 11	Jul 13	Aug 27-Oct 01
		July	TM0CE7	8	Mar 25	May 21	Jun 23	Jul 18	Jul 20	Sep 07-Oct 12
		August	TM0CE8	6	Apr 28	Jun 25	Jul 28	Aug 21	Aug 24	Oct 08-Nov 12
		October	TM0CF1	6	Jun 25	Aug 27	Sep 29	Oct 24	Oct 26	Dec 10-Jan 14 2028
		November	TM0CF3	8	Jul 27	Sep 10	Oct 13	Nov 7	Nov 9	Dec 29-Feb 01 2028
		November	TM0CF2	3	Jul 27	Sep 24	Oct 27	Nov 21	Nov 23	Jan 07-Feb 11 2028

* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.

** SSMC does not tape-out of a GDS that includes Embedded OTP/MTP.

0.18um High Voltage BCD (Generation-2 & 3), 5V flavors & SiGe

Technology	Flavor	Month	Shuttle Ref	Fab	Reserve before	Purchase order before	Dry run GDS	Final GDS*	Tape-out	Estimated shipment date
0.18um	High Voltage, BCD (Generation-2)	January	TM0CE1	8	Oct 5 2026	Nov 20 (2026)	Dec 23 2026	Jan 17	Jan 19	Mar 31-May05
		March	TM0CE2	SSMC**	Nov 25 2026	Jan 8	Feb 10	Mar 7	Mar 9	Jun 01-Jul 06
		April	TM0CE3	6	Dec 28 2026	Feb 26	Mar 31	Apr 25	Apr 27	Jul 07-Aug 11
		May	TM0CE4	3	Jan 27	Mar 26	Apr 28	May 23	May 25	Jul 31-Sep 04
		July	TM0CE7	8	Mar 25	May 21	Jun 23	Jul 18	Jul 20	Sep 25-Oct 30
		August	TM0CE8	6	Apr 28	Jun 25	Jul 28	Aug 22	Aug 24	Oct 30-Dec 04
		September	TM0CE9	SSMC**	May 25	Jul 09	Aug 11	Sep 05	Sep 07	Nov 30-Jan 04 2028
		September	TM0CF0	3	May 25	Jul 30	Sep 01	Sep 26	Sep 28	Dec 04-Jan 08 2028
		October	TM0CF1	6	Jun 25	Aug 27	Sep 29	Oct 24	Oct 26	Jan 02-Feb 05 2028
		November	TM0CF3	8	Jul 27	Sep 10	Oct 13	Nov 7	Nov 9	Jan 15-Feb 19 2028
	High Voltage, BCD (Generation-3)	January	TM0CE1	8	Oct 5 2026	Nov 20 (2026)	Dec 23 2026	Jan 17	Jan 19	Apr 03-May 08
		March	TM0CE2	SSMC**	Nov 25 2026	Jan 8	Feb 10	Mar 7	Mar 9	Jun 03-Jul 08
		April	TM0CE3	6	Dec 28 2026	Feb 26	Mar 31	Apr 25	Apr 27	Jul 10-Aug 14
		July	TM0CE7	8	Mar 25	May 21	Jun 23	Jul 18	Jul 20	Sep 29-Nov 03
		August	TM0CE8	6	Apr 28	Jun 25	Jul 28	Aug 22	Aug 24	Nov 03-Dec 08
		September	TM0CE9	SSMC**	May 25	Jul 09	Aug 11	Sep 05	Sep 07	Dec 02-Jan 06 2028
		October	TM0CF1	6	Jun 25	Aug 27	Sep 29	Oct 24	Oct 26	Jan 05-Feb 09 2028
		November	TM0CF3	8	Jul 27	Sep 10	Oct 13	Nov 7	Nov 9	Jan 19-Feb 23 2028
		January	TM0CE1	8	Oct 05 2026	Nov 20 2026	Dec 22 2026	Jan 17	Jan 19	Mar 09-Apr 13
0.18um	Mixed Signal, G, (1.8/5V)	March	TM0CE2	SSMC**	Nov 25 2026	Jan 08	Feb 10	Mar 07	Mar 09	May 11-Jun 15
		July	TM0CE7	8	Mar 25	May 21	Jun 23	Jul 18	Jul 20	Sep 07-Oct 12
		September	TM0CE9	SSMC**	May 25	Jul 09	Aug 11	Sep 05	Sep 07	Nov 09-Dec 14
		November	TM0CF3	8	Jul 27	Sep 10	Oct 13	Nov 7	Nov 9	Dec 28-Feb 01 2028
		January	TM0CE1	8	Oct 05 2026	Nov 20 2026	Dec 22 2026	Jan 17	Jan 19	Mar 09-Apr 13
	Mixed Signal, GPIA, (1.8/5V)	July	TM0CE7	8	Mar 25	May 21	Jun 23	Jul 18	Jul 20	Sep 07-Oct 12
		November	TM0CF3	8	Jul 27	Sep 10	Oct 13	Nov 7	Nov 9	Dec 28-Feb 01 2028
	SiGe BiCMOS, G (1.8/3.3V)	July	TM0CE6	3	Mar 25	May 14	Jun 14	Jul 11	Jul 13	Sep 26-Oct 27

* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.

**SSMC does not tape-out of a GDS that includes Embedded OTP/MP

0.25um ~ 0.35um

Technology	Flavor	Month	Shuttle Ref	Fab	Reserve before	Purchase order before	Dry run GDS	Final GDS*	Tape-out	Estimated shipment date
0.25um	Logic, G (2.5/3.3V, 2.5/5V)	March	TM0CD9	8	Nov 25 2026	Jan 22	Feb 24	Mar 21	Mar 23	May 07-Jun 11
	Mixed-Signal/RF, G (2.5/3.3V, 2.5/5V)	September	TM0CE0	10	May 25	Jul 9	Aug 11	Sep 5	Sep 7	Oct 30-Dec 04
	High Voltage BCD (2.5/5/12/24/40V/Vg2.5/5V) High Voltage BCD (2.5/5/12/24/40/Vg2.5/5/12V) High Voltage Gen2 BCD (2.5/5/7/12/20/24/40/45/60V/Vg 2.5/5/12V)	March	TM0CD9	8	Nov 25 2026	Jan 22	Feb 24	Mar 21	Mar 23	May 28-Jul 02
	High Voltage BCD (2.5/5/60V/Vg 2.5/5V) High Voltage BCD (2.5/5/12/24/40/60/Vg2.5/5/12V)	March	TM0CD9	8	Nov 25 2026	Jan 22	Feb 24	Mar 21	Mar 23	May 28-Jul 02
0.35um	High Voltage BCD (3.3/20/23/Vg3.3V)	May	TM0C79	3	Jan 27	Mar 26	Apr 28	May 23	May 25	Jul 12-Aug 16
	High Voltage BCD (3.3/5/12/15/20/40/Vg3.3/5/12V)	May	TM0C79	3	Jan 27	Mar 26	Apr 28	May 23	May 25	Jul 12-Aug 16
	High Voltage, G, DDD (3.3/12/13.5)	May	TM0C79	3	Jan 27	Mar 26	Apr 28	May 23	May 25	Jul 12-Aug 16
	Logic, G, Polycide/Silicide (3.3/5V) Mixed-Signal, G (3.3/5V)	May	TM0C79	3	Jan 27	Mar 26	Apr 28	May 23	May 25	Jul03-Aug 07

CyberShuttle reservation & design delivery information

- Single reservation for multiple chips
- No backup reservation
- Provide single GDS with all designs,
 - Enclosed with TSMC searing + 80um scribe (post-shrink if applicable).
 - If designs are not identical, put marker in the scribe line.
 - Add dummies to the scribe line for 12-inch tape-outs.
 - Exception: multiple reservations accepted for different projects with different metal stacks or far backend.

CyberShuttle cycle time

- The estimated shipment date is applicable for reservations with quantity <200 dies.
- If additional samples are required, additional cycle time of (1~3 weeks) might be needed.
- Cycle time estimates are based on typical conditions. Corner wafers or SHDMiM processing requires additional time.
- Optional services adding cycle time
 - Wafer thinning smaller than 10mils: up to 12 days
 - Additional bumped wafer thinning and die saw (each 200 ea.): 5 working days

TSMC CyberShuttle – IP merge guidelines

To ensure timely inclusion in the TSMC CyberShuttle when an IP merge is required, deliver the final GDS 2 weeks in advance to allow sufficient time for integration and validation.

Why This Matters:

- **Complete LVS Setup Required**

A fully validated LVS setup must be in place before initiating the merge process.

- **Ip-transfer**

Third-party IPs have to be transferred from the vendor to the TSMC merge team, which may introduce delays in the process.

- **Increased Complexity with Multiple IP Instances**

Merging several IP blocks adds significant complexity and increases the risk of integration issues.

- **Merge Errors Can Jeopardize the Deadline**

Errors discovered after merging may delay the process and reduce the likelihood of meeting the shuttle schedule. TSMC requests to re-submit the merge even for minor typos or missing files

Questions? Contact us at

eptsmc@imec.be

For support on the tape-out submission

salesops@imec.be

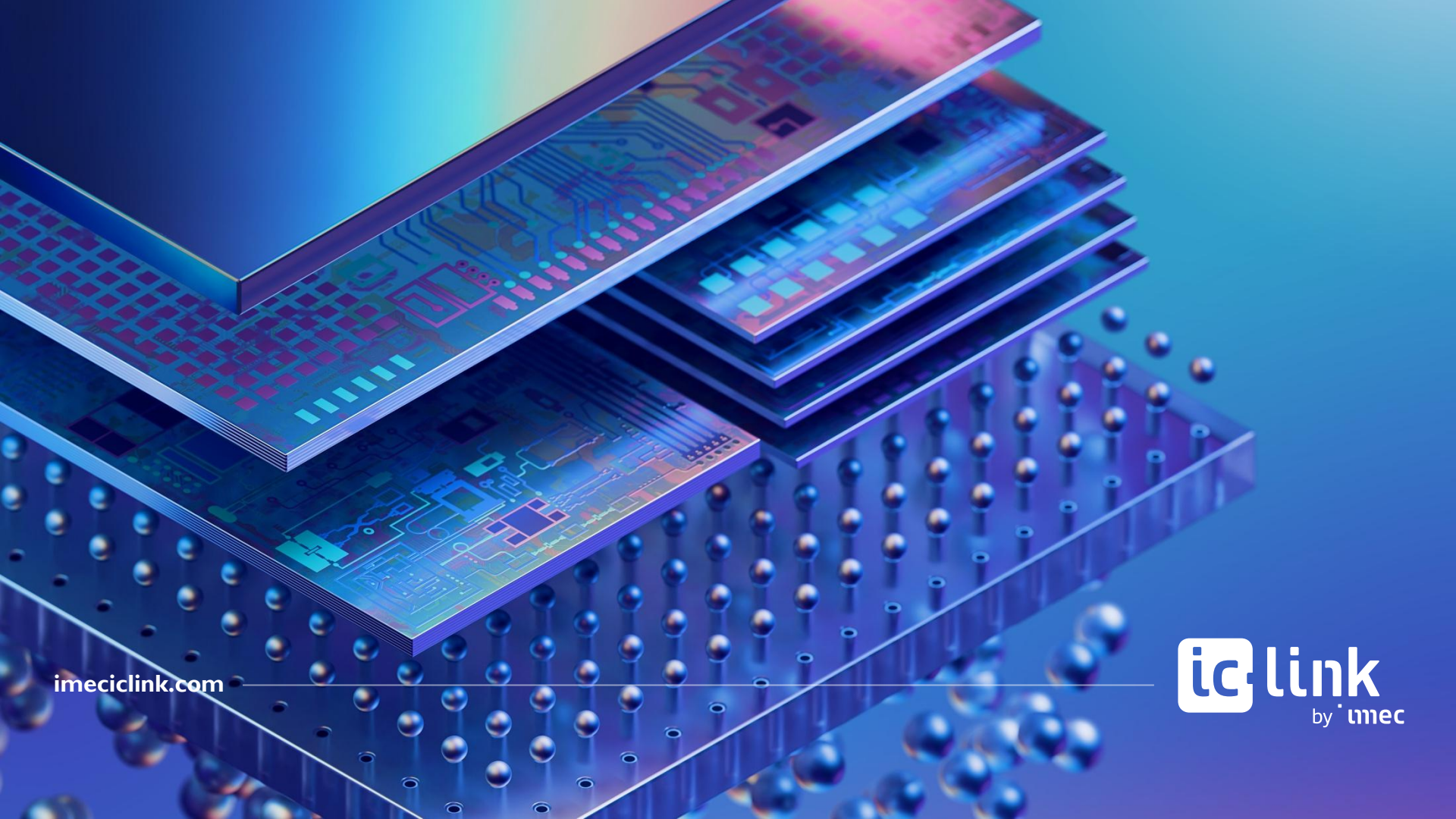
For quotations

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For support on export documents and purchase orders

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For support on foundry libraries, PDK's (installation, flavors, bugs, ...), LVS



imeciclink.com

ic link
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