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DARE - radiation hardening by design

DARE22G

0.8 V Voltage Monitor

Product Brief

Product Overview

DARE22G VMON08 implements a 0.8 V voltage monitor for radiation-hardened applications in the commercial GF 22 nm FDSOI CMOS technology.

Features

Main functionalities include:

- Digital calibration with 16 trimming points
- Low static current consumption (< 50 µA)
- 25 mV hysteresis (typical)
- TID immunity over 100 krad (SiO_2)
- SET immunity over 60 MeV.cm^2/mg
- SEL immunity over 70 MeV.cm^2/mg

Radiation Hardening

DARE22G VMON08 exploits the intrinsic SEL immunity provided by the FDSOI technology in combination with special radiation-hardening-by-design (RHBD) techniques to mitigate TID and single-event effects.

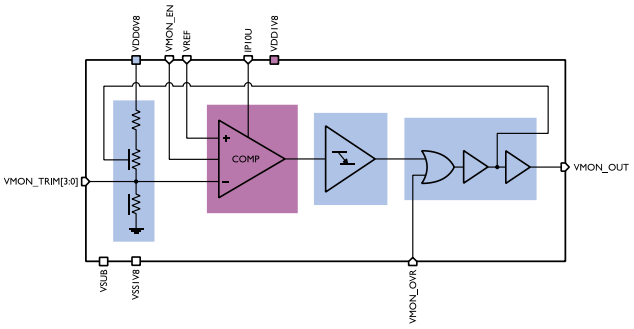
Block Diagram

The VMON08 macro consists of a digitally controlled resistive divider, a comparator, a level shifter, and digital buffers, all arranged in a feedback loop to create hysteresis.

The integrated comparator requires an external high-accuracy 10 µA sinking current source and a 0.6 V reference voltage to operate. These signals can be provided on-chip by the DARE22G IVREF18 IP.

The voltage status output switches to 1 once the input reference voltage and all power supplies are stable.

Digital calibration is supported by input trimming bits controlling the internal resistive divider.



Pin Interface

Pin Name	Type	Description
VDD1V8	Power	I/O power supply
VDD0V8	Power	Core power supply
VSS1V8	Ground	Ground supply
VSUB	Ground	P-substrate bias voltage
VREF	Analog	0.6 V reference voltage
IP10U	Analog	10 µA bias current
VMON_OUT	Digital	Output status
VMON_EN	Digital	Enable
VMON_OVR	Digital	Output override
VMON_TRIM[3:0]	Digital	Trimming bits

Physical Dimensions

DARE22G VMON08 is implemented as a core macro.

IP Name	Width	Height
VMON08	125 µm	40 µm

Contact

For further information, please contact us at dare@imec.be

Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	Minimum	Typical	Maximum	Unit
Core supply voltage	V_{DD0V8}	0.72	0.8	0.88	V
I/O supply voltage	V_{DD1V8}	1.62	1.8	1.98	V
Operating temperature	T_J	-40	25	125	°C
TID threshold	TID_{th}	100			krad (SiO_2)
LET threshold (SET)	LET_{th_SET}	60			MeV.cm^2/mg
LET threshold (SEL)	LET_{th_SEL}	70			MeV.cm^2/mg