DARE22G
1.2 V SSTL Library
Product Brief

Product Overview

DARE22G SSTL12 library provides single-ended and differential transceiver I/O cells for the implementation of radiation-hardened DDR4 interfaces in the commercial GF 22 nm FDSOI CMOS technology.

DARE22G SSTL12 interfaces are fully compliant with the DDR4 standard and can achieve data signaling rates up to 3.2 Gbit/s. Different configurations for transmitter drivers (R_{ON}) and receiver on-die terminations (ODT) are supported.

Features

Main features include:

- 1.2 V I/O supply domain cells
- Pad-limited fixed-height narrow layout
- Distributed power-on control
- Cold spare functionality
- 2 kV ESD protection (HBM)
- SET immunity over 60 MeV.cm^2/mg
- SEL immunity over 70 MeV.cm^2/mg
- TID immunity over 100 krad (SiO_2)

DARE22G SSTL12 library includes all support cells, such as voltage reference generators, adapters, and supply cells, required to implement SSTL domains compatible with DARE22G I/O rings.

Radiation Hardening

DARE22G SSTL12 cells exploit the intrinsic SEL immunity of the FDSOI process in combination with various radiation-hardening-by-design (RHBD) techniques to mitigate TID and single-event effects.

SSTL Transceivers

Transceivers cells are available in both single-ended (RXTX_SE) and differential (RXTX_DIFF) variations. These I/O cells can be configured to operate in either transmitter or receiver mode.

Cell Features

SSTL12_RXTX main functionalities include:

- Data transfer rates up to 3.2 Gbit/s
- Power-down mode (< 80 µA)
- Two driving capabilities R_{ON} (34 and 40 Ω)
- Multiple ODT configurations (34 to 240 Ω)
- Digital R_{ON}/ODT calibration for process variation compensation
- Configurable reference voltage (0.65 to 1.19 V)
- Pseudo-Open Drain for low power consumption

Pin Interface

Pin Name	Type	Description
VDDIO	Power	I/O power supply
VSSIO	Ground	I/O ground supply
VDDC	Power	Core power supply
VSSC	Ground	Core ground supply
VREF	Analog	Internal reference voltage
PWROK	Analog	Core supply voltage flag
PDB	Digital	Power-down enable
DS[2:0]	Digital	Impedance selection
ZQ_TUNE [2:0]	Digital	ODT calibration bits
DIN	Digital	TX core input
PADN PADP	SSTL	TX outputs or RX inputs (differential cell)
PAD	SSTL	TX output or RX input (single-ended cell)
DOUT	Digital	RX core output

Physical Dimensions

DARE22G SSTL12 cells are implemented in a pad-limited fixed-height narrow layout configuration compatible with the DARE22G I/O library specifications.

Cell Name	Width	Height
SSTL12_RXTX_SE	150 µm	89 µm
SSTL12_RXTX_DIFF	300 µm	89 µm

Contact

For further information, please contact us at
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Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	Minimum	Typical	Maximum	Unit
Core supply voltage	V_{DD0V8}	0.72	0.8	0.88	V
I/O supply voltage	V_{DD1V2}	1.14	1.2	1.26	V
Operating temperature	T_J	-40	25	125	°C
ESD rating (HBM)	V_{HBM}	2			kV
TID threshold	TID_{th}	100			krad (SiO_2)
LET threshold (SET)	LET_{th_SET}	60			MeV.cm^2/mg
LET threshold (SEL)	LET_{th_SEL}	70			MeV.cm^2/mg