# DARE22G
## 1.8 V Power-On-Reset
Product Brief

## Product Overview

DARE22G POR18 implements a 1.8 V supply power-on-reset circuit for radiation-hardened applications in the commercial GF 22 nm FDSOI CMOS technology.

This IP macro supports a range of DARE22G platform IP blocks that require power-on-reset signals in the 1.8 V supply domain.

## Features

Main functionalities include:

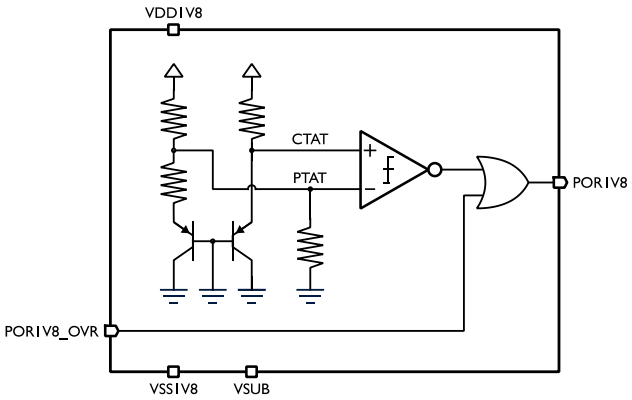
- 1.8 V output reset signal
- External reset assertion override
- Positive-going trip point range of 1.36 – 1.42 V
- Negative-going trip point range of 1.36 – 1.40 V
- Hysteresis range of 0 – 40 mV
- Low operating current (≤ 8 µA)
- TID immunity over 100 krad ($SiO_2$)
- SET immunity over 60 MeV.cm$^2$/mg
- SEL immunity over 70 MeV.cm$^2$/mg

## Block Diagram

The POR18 macro generates a reset signal when the 1.8 V power supply is first applied to the chip and keeps it asserted until the supply voltage reaches its nominal value. It employs a bandgap-based architecture, where PTAT and CTAT voltages from an open-loop bandgap reference are compared to produce the power-on reset signal.

The internally generated reset signal in the 1.8 V domain is output via the POR1V8 pin.

The power-on reset functionality can be combined with an external 1.8 V reset signal provided via the POR1V8_OVR pin. When asserted, this input signal will override the internally generated reset signal.




## Pin Interface

| Pin Name | Type | Description |
|---|---|---|
| VDD1V8 | Power | Power supply |
| VSS1V8 | Ground | Ground supply |
| VSUB | Ground | P-substrate bias voltage |
| POR1V8 | Digital | Reset output |
| POR1V8_OVR | Digital | Reset override input |

## Physical Dimensions

DARE22G POR18 is implemented as a core macro.

| IP Name | Width | Height |
|---|---|---|
| POR18 | 58 µm | 263 µm |

## Contact

For further information, please contact us at
dare@imec.be

## Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

| Parameter | Name | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD1V8}$ | 1.62 | 1.8 | 1.98 | V |
| Operating temperature | $T_J$ | -40 | 25 | 125 | °C |
| TID threshold | $TID_{th}$ | 100 | | | krad ($SiO_2$) |
| LET threshold (SET) | $LET_{th\_SET}$ | 60 | | | MeV.cm$^2$/mg |
| LET threshold (SEL) | $LET_{th\_SEL}$ | 70 | | | MeV.cm$^2$/mg |