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DARE - radiation hardening by design

DARE22G

Phase-Locked Loop

Product Brief

Product Overview

DARE22G PLL implements a complete radiation-hardened phase-locked loop IP in the commercial GF 22 nm FDSOI CMOS technology.

Features

Main functionalities include:

- Wide output frequency range (1.953 MHz – 3 GHz)
- Wide input frequency range (20 MHz – 800 MHz)
- Programmable input and output clock dividers
- Built-in clock generation bypassing
- Built-in digital lock detection
- Low RMS period jitter below 1 ps
- Power-down mode (< 7 µA)
- Maximum current consumption below 30 mA
- SET immunity over 60 MeV.cm^2/mg
- SEL immunity over 70 MeV.cm^2/mg
- TID tolerance over 100 krad (SiO_2)

Radiation Hardening

DARE22G PLL exploits the intrinsic SEL immunity of the FDSOI process in combination with various radiation-hardening-by-design (RHBD) techniques to mitigate TID and single-event effects.

Strong drive-strength gates, SET filters, and redundancy techniques are employed in digital and analog circuitry to achieve SEE immunity for LET levels over 60 MeV/cm^2.mg.

Block Diagram

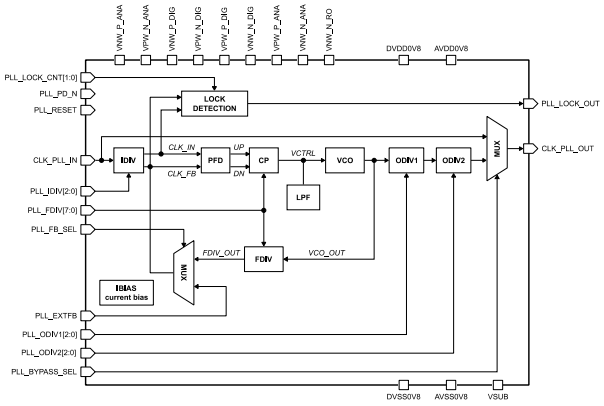
The core of the PLL macro is composed of a TMR-hardened VCO, a programmable charge pump synchronized with a feedback frequency divider, a PFD, and a second-order LPF. A current bias circuit provides a reference current to the charge pump.

The input clock signal is scaled by the input divider (IDIV) to match the feedback clock signal frequency which is derived from the VCO clock signal after the feedback divider (FDIV) in the PLL core. These two signals are inputs to both the PFD and the lock detection circuits.

The digital lock detection mechanism provides an output flag signal that raises to 1 when input and output clock signals are phase-synchronized.

Two additional dividers (ODIV1 & ODIV2) connected in series are used to derive the output clock signal from the VCO output at the desired frequency.

A multiplexer before the clock output pin allows the selection between the generated clock and the input clock signals via an input control signal. Bypassing the generated clock may be useful during initialization or reconfiguration while waiting until the lock state is achieved.



Pin Interface

Pin Name	Type	Description
AVDD0V8	Power	Analog power supply
AVSS0V8	Ground	Analog ground supply
DVDD0V8	Power	Digital power supply
DVSS0V8	Ground	Digital ground supply
CLK_PLL_IN	Digital	Reference input clock
CLK_PLL_OUT	Digital	Output clock
PLL_BYPASS_SEL	Digital	Bypass-mode enable
PLL_EXTFB	Digital	External feedback clock
PLL_FB_SEL	Digital	Feedback clock selection
PLL_FDIV[7:0]	Digital	Selection bits for FDIV's division factor
PLL_IDIV[2:0]	Digital	Selection bits for IDIV's division factor
PLL_LOCK_CNT[1:0]	Digital	Lock detection counter selection bits
PLL_LOCK_OUT	Digital	Lock detection flag
PLL_ODIV1[2:0]	Digital	Selection bits for ODIV1's division factor
PLL_ODIV2[2:0]	Digital	Selection bits for ODIV2's division factor
PLL_PD_N	Digital	Power-down enable
PLL_RESET	Digital	Reset for digital blocks
VNW_N_ANA	Ground	N-well forward-body voltage for analog blocks
VNW_N_DIG	Ground	N-well forward-body voltage for digital blocks
VNW_N_RO	Power	N-well forward-body voltage for VCO
VNW_P_ANA	Ground	N-well reverse-body voltage for analog blocks
VNW_P_DIG	Power	N-well reverse-body voltage for digital blocks
VPW_N_ANA	Ground	P-well reverse-body voltage for analog blocks
VPW_N_DIG	Ground	P-well reverse-body voltage for digital blocks
VPW_P_ANA	Ground	P-well forward-body voltage for analog blocks
VPW_P_DIG	Power	P-well forward-body voltage for digital blocks
VSUB	Ground	P-substrate bias voltage

Physical Dimensions

DARE22G PLL is implemented as a core macro.

IP Name	Width	Height
PLL	1140 µm	603 µm

Contact

For further information, please contact us at
dare@imec.be

Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	Minimum	Typical	Maximum	Unit
Analog supply voltage	V_{AVDD}	0.72†	0.8	0.88	V
Digital supply voltage	V_{DVDD}	0.72†	0.8	0.88	V
Operating temperature	T_J	-40	25	125	°C
TID threshold	TID_{th}	100			krad (SiO_2)
LET threshold (SET)	LET_{th_SET}	60			MeV.cm^2/mg
LET threshold (SEL)	LET_{th_SEL}	70			MeV.cm^2/mg

† Minimum analog & digital supply voltage is specified at 0.76 V for maximum VCO frequency of 3 GHz