DARE22G
100 MHz Oscillator
Product Brief

Product Overview

DARE22G OSC100M implements a current-capacitor relaxation oscillator for radiation-hardened applications in the commercial GF 22 nm FDSOI CMOS technology.

Features

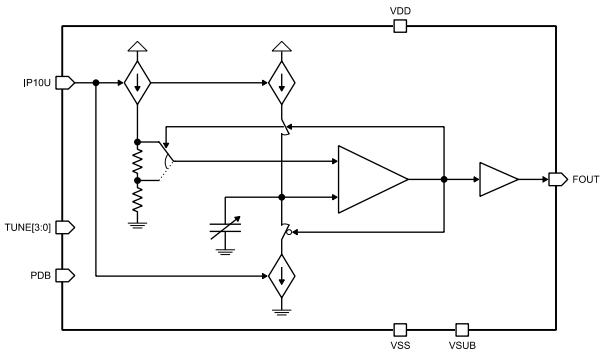
Main functionalities include:

- 100 MHz base output frequency (± 4%)
- 4-bit trimming calibration
- 92 – 112 MHz output frequency range over corners after calibration
- Maximum SET-induced jitter of 2.8 ns
- Power-down mode (< 1 µA)
- Max current consumption below 250 µA
- TID immunity over 100 krad (SiO_2)
- SET immunity over 60 MeV.cm^2/mg
- SEL immunity over 70 MeV.cm^2/mg

Block Diagram

The OSC100M macro cell mainly consists of a comparator and a tunable capacitor that is sequentially charged and discharged to produce an oscillating signal.

Charge and discharge cycles are controlled by the comparator using reference voltage levels generated through two internal resistors. Reference voltage generation and charging/discharging circuitry require a 10 µA sinking current source connected to the IP10U input. This signal can be provided on-chip by the DARE22G IVREF18 IP.



Pin Interface

Pin Name	Type	Description
VDD	Power	Power supply
VSS	Ground	Ground supply
VSUB	Ground	P-substrate bias voltage
IP10U	Analog	10 µA current reference
PDB	Digital	Active-low power-down enable
TUNE[3:0]	Digital	Frequency tuning bits
FOUT	Digital	Output clock

Physical Dimensions

DARE22G OSC100M is implemented as a core macro.

IP Name	Width	Height
OSC100M	68 µm	69 µm

Contact

For further information, please contact us at
dare@imec.be

Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	Minimum	Typical	Maximum	Unit
Supply voltage	V_{DD}	0.72	0.8	0.88	V
Input reference current	I_{P10U}	9	10	11	µA
Operating temperature	T_J	-40	25	125	°C
ESD rating (HBM)	V_{HBM}	2			kV
TID threshold	TID_{th}	100			krad (SiO_2)
LET threshold (SET)	LET_{th_SET}	60			MeV.cm^2/mg
LET threshold (SEL)	LET_{th_SEL}	70			MeV.cm^2/mg