Product Overview

DARE22G LVDS library provides transmitter and receiver I/O cells for the implementation of radiation-hardened high-speed low-voltage differential signaling interfaces in the commercial GF 22 nm FDSOI CMOS technology.

DARE22G LVDS interfaces are fully compliant with the TIA/EIA-644-A standard and can achieve data signaling rates up to 1 Gbit/s. Special capabilities for space applications are built in transmitter and receiver cells, including on-chip hysteresis, cold-spare functionality, and radiation-hardened fail-safe detection.

Features

DARE22G LVDS library features include:

- 1.8 V I/O supply voltage
- Pad-limited fixed-height narrow layout
- Distributed power-on control
- Horizontal or vertical placement orientation
- Inline and staggered pad arrangement supported
- 2 kV ESD protection (HBM)
- TID immunity over 100 krad (SiO_2)
- SET immunity over 60 MeV.cm^2/mg
- SEL immunity over 70 MeV.cm^2/mg

Radiation Hardening

DARE22G LVDS cells exploit the intrinsic SEL immunity of the FDSOI process in combination with various radiation-hardening-by-design (RHBD) techniques to mitigate TID and single-event effects.

LVDS Transmitter

The LVDS transmitter cell (LVDS_TX) converts a single-ended digital core signal into a low-voltage differential output signal centered around a common-mode voltage supplied by the chip core.

Cell Features

LVDS_TX main functionalities include:

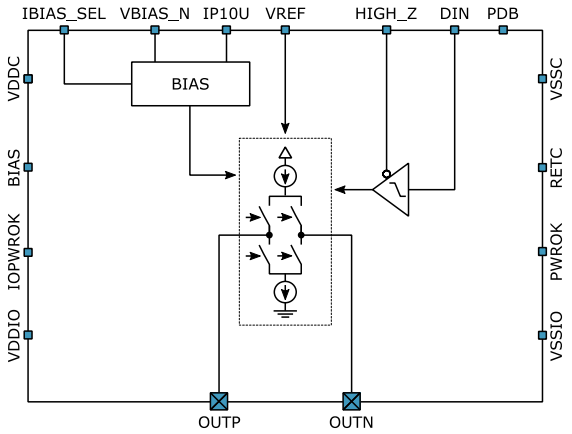
- High-impedance output mode to enable multipoint configurations with multiple transmitters
- Power-down mode (< 85 µA)
- Disabled data outputs during power ramping
- Variable common-mode voltage
- Flexible reference biasing
- Cold-spare compliant outputs
- Maximum current consumption of 5.8 mA at 1 Gbps
- SET immunity above 60 MeV.cm^2/mg

The output common-mode voltage is generated from a 1.25 V (±5%) voltage reference, which must be provided via a core-side input pin.

LVDS_TX is not self-biased and requires a reference signal to be supplied via core pins to bias its internal current mirrors. This biasing can be implemented using either current or voltage signals. In current-signal mode, a 10 µA sinking current signal must be provided. Transmitter cells biased this way will generate a voltage reference signal that can be redistributed to bias additional **transmitter** cells in voltage-signal mode. This flexibility is intended to reduce power requirements. Fully on-chip biasing is supported by the DARE22G IVREF18 IP.

LVDS_TX is designed to achieve maximum performance with a 100 Ω termination resistor load, following the reference specification established by the TIA/EIA-644-A industry standard.

Block Diagram



Pin Interface

Pin Name	Type	Description
VDDIO	Power	I/O power supply
VSSIO	Ground	I/O ground supply
VDDC	Power	Core power supply
VSSC	Ground	Core ground supply
IP10U	Analog	Single-cell bias current
VBIAS_N	Analog	Shared bias voltage
VREF	Analog	Common-mode reference voltage
IOPWROK	Digital	I/O supply voltage flag
PWROK	Digital	Core supply voltage flag
RETC	Digital	Retention enable
BIAS	Digital	Level-shifter bias voltage
IBIAS_SEL	Digital	Current biasing selection
PDB	Digital	Power-down enable
DIN	Digital	Single-ended input data
HIGH_Z	Digital	Tri-state output enable
OUTP OUTN	LVDS	Differential output data

LVDS Receiver

The LVDS receiver cell (LVDS_RX) converts an external low-voltage differential signal with a variable common-mode voltage into a single-ended digital core output signal.

Cell Features

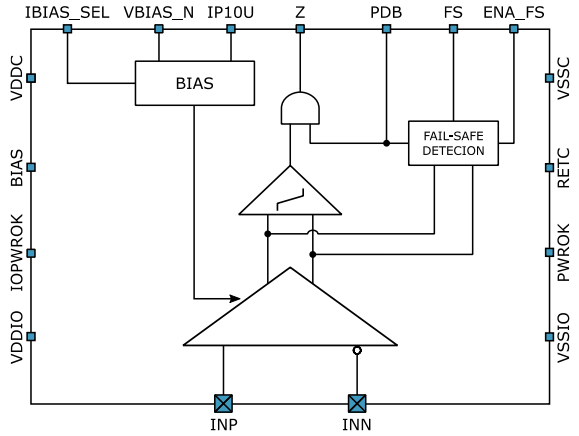
LVDS_RX main functionalities include:

- Active fail-safe detection
- Power-down mode (< 10 µA)
- Pulled down data output during power ramping
- Flexible reference biasing
- Cold-spare compliant inputs
- Maximum current consumption of 3.2 mA at 1 Gbps
- SET immunity over 60 MeV.cm^2/mg

LVDS_RX is not self-biased and requires a reference signal to be supplied via core pins to bias its internal current mirrors. This biasing can be implemented using either current or voltage signals. In current-signal mode, a 10 µA sinking current signal must be provided. Receiver cells biased this way will generate a voltage reference signal that can be redistributed to bias additional **receiver** cells in voltage-signal mode. This flexibility is intended to reduce power requirements. Fully on-chip biasing is supported by the DARE22G IVREF18 IP.

Integrated fail-safe detection can be enabled to flag invalid input conditions, such as open-circuit, short-circuit, or high-impedance states. When a failure is detected, the fail-safe flag output to the core is asserted, while the data output remains unaffected.

Block Diagram



Pin Interface

Pin Name	Type	Description
VDDIO	Power	I/O power supply
VSSIO	Ground	I/O ground supply
VDDC	Power	Core power supply
VSSC	Ground	Core ground supply
IP10U	Analog	Single-cell bias current
VBIAS_N	Analog	Shared bias voltage
IOPWROK	Digital	I/O supply voltage flag
PWROK	Digital	Core supply voltage flag
RETC	Digital	Retention enable
BIAS	Digital	Level-shifter bias voltage
IBIAS_SEL	Digital	Current biasing selection
PDB	Digital	Power-down enable
ENA_FS	Digital	Fail-safe enable
FS	Digital	Fail-safe detection flag
Z	Digital	Single-ended output data
INP INN	LVDS	Differential input data

Physical Dimensions

DARE22G LVDS cells are implemented in a pad-limited fixed-height narrow layout configuration compatible with the DARE22G I/O library specifications.

Cell Name	Width	Height
LVDS_RX	203 µm	89 µm
LVDS_TX	185 µm	89 µm

Contact

For further information, please contact us at
dare@imec.be

Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	Minimum	Typical	Maximum	Unit
Core supply voltage	V_{DD0V8}	0.72	0.8	0.88	V
I/O supply voltage	V_{DD1V8}	1.62	1.8	1.98	V
Core input voltage	V_{CORE}	-0.3		0.88	V
Pad input voltage	V_{PAD}	0		2.4	V
Reference voltage	V_{REF}		1.25		V
Bias current	I_{BIAS}	9	10	11	µA
Operating temperature	T_J	-40	25	125	°C
ESD rating (HBM)	V_{HBM}	2			kV
TID threshold	TID_{th}	100			krad (SiO_2)
LET threshold (SET)	LET_{th_SET}	60			MeV.cm^2/mg
LET threshold (SEL)	LET_{th_SEL}	70			MeV.cm^2/mg