DARE22G

1.8 V Current & Voltage Reference

Product Brief

Product Overview

DARE22G IVREF18 implements a bandgap-based reference voltage and current generator for radiation-hardened applications in the commercial GF 22 nm FDSOI CMOS technology.

This IP macro supports a range of DARE22G platform IP blocks that require on-chip current and/or voltage biasing, such as LVDS, BBG, and OSC100M.

Features

Main functionalities include:

- 0.6 V and 1.25 V (±1%) reference voltages
- 10 µA high-accuracy current sources (10 replicas)
- 10 µA internal biasing current sources for external reference voltage generation (9 replicas)
- Excellent stability over supply voltage, load variation and temperature
- Low operating current (< 420 µA)
- Digital calibration
- Power-down mode (< 1 µA)
- TID immunity over 100 krad (SiO_2)
- SET immunity over 60 MeV.cm^2/mg
- SEL immunity over 70 MeV.cm^2/mg

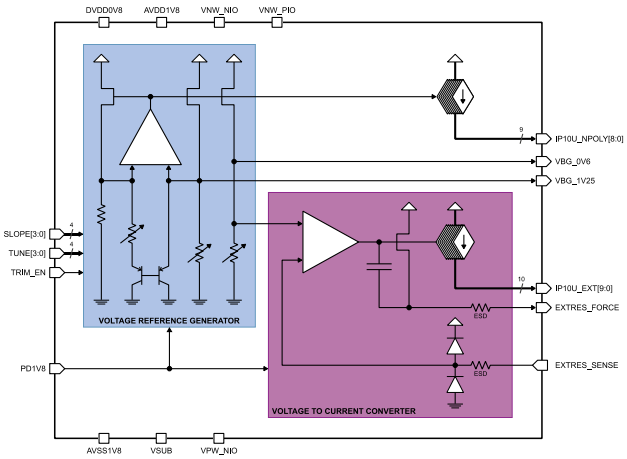
Block Diagram

The IVREF18 macro comprises a bandgap circuit, current mirrors, and a voltage-to-current converter. The bandgap circuit generates 0.6 V and 1.25 V reference voltage signals which are output through the VBG_0V6 and VBG_1V25 pins, respectively. Digital calibration for voltage offset and temperature drift can be performed using trimming codes provided via the TUNE[3:0] and SLOPE[3:0] input buses. Calibration is enabled when the TRIM_EN input is asserted during start-up.

The voltage-to-current converter uses internal reference voltage signals to generate high-accuracy 10 µA current source replicas, which are output via the IP10U_EXT[9:0] bus. This functionality requires an external pull-down resistor connected to both EXTRES_FORCE and EXTRES_SENSE pins. Additionally, integrated current mirrors replicate the internal bandgap biasing current to deliver several 10 µA biasing current sources via the IP10U_NPOLY[8:0] output bus.

High-accuracy current sources are designed for general applications and rely on an accurate external resistor, which is usually practical only off-chip. In contrast, internal biasing current sources offer a fully integrated alternative that requires no external components. These current sources are more sensitive to PVT variations but can be paired with dedicated NPOLY resistors to create accurate reference voltage signals in external circuits.

Output current source replicas allow multiple blocks to be biased from a single IVREF18 instance.



Pin Interface

Pin Name	Type	Description
AVDD1V8	Power	Analog power supply
DVDD0V8	Power	Digital power supply
AVSS1V8	Ground	Ground supply
VSUB	Ground	P-substrate bias voltage
VNW_PIO	Power	Back-bias voltage for reversed-biased NMOS
VNW_NIO	Power	Back-bias voltage for forward-biased NMOS
VPW_NIO	Ground	Back-bias voltage for reversed-biased PMOS
VBG_0V6	Analog	0.6 V reference voltage
VBG_1V25	Analog	1.25 V reference voltage
IP10U_NPOLY[8:0]	Analog	10 µA internal biasing current sources
IP10U_EXT[9:0]	Analog	10 µA high-accuracy current sources
EXTRES_FORCE	Analog	External 12 kΩ resistor low-ohmic connection
EXTRES_SENSE	Analog	External 12 kΩ resistor sensing connection
PD1V8	Digital	Power-down enable
TUNE[3:0]	Digital	Offset trimming bits for reference voltages
SLOPE[3:0]	Digital	Temperature slope trimming bits for reference voltages
TRIM_EN	Digital	Trimming enable

Physical Dimensions

DARE22G IVREF18 is implemented as a core macro.

IP Name	Width	Height
IVREF18	526 µm	220 µm

Contact

For further information, please contact us at dare@imec.be

Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	Minimum	Typical	Maximum	Unit
Digital supply voltage	V_{DD0V8}	0.72	0.8	0.88	V
Analog supply voltage	V_{DD1V8}	1.62	1.8	1.98	V
Operating temperature	T_J	-40	25	125	°C
ESD rating (HBM)	V_{HBM}	2			kV
TID threshold	TID_{th}	100			krad (SiO_2)
LET threshold (SET)	LET_{th_SET}	60			MeV.cm^2/mg
LET threshold (SEL)	LET_{th_SEL}	70			MeV.cm^2/mg