Product Overview

DARE22G provides a set of standard cell libraries for the implementation of radiation-hardened digital logic circuits in the commercial GF 22 nm FDSOI CMOS technology.

Each library variant implements the same cell set using a different combination of Vt flavor and gate length to provide distinct speed and leakage trade-offs that can be further adjusted via back-gate bias voltage tuning.

Vt Flavor	Gate Length	Well Structure
SLVT	20 nm	FBB (flip well)
SLVT	24 nm	FBB (flip well)
SLVT	28 nm	FBB (flip well)
LVT	20 nm	FBB (flip well)
LVT	24 nm	FBB (flip well)
LVT	28 nm	FBB (flip well)
RVT	20 nm	RBB (conventional well)
RVT	24 nm	RBB (conventional well)
RVT	28 nm	RBB (conventional well)
HVT	20 nm	RBB (conventional well)
HVT	24 nm	RBB (conventional well)
HVT	28 nm	RBB (conventional well)

All libraries are based on a common layout template supporting mixed integration of matching-well variants within the same standard cell implementation. Equivalent cells across different library variants feature identical footprints to enable post-layout design optimizations via cell replacement without additional place & route iterations.

Library Cells

DARE22G standard cell libraries include the following categories of cells:

- Non-hardened combinational
- Non-hardened sequential
- SET-hardened combinational
- SEU-hardened sequential
- TMR enablement
- P&R enablement

Radiation Hardening

DARE22G exploits the intrinsic SEL immunity of the FDSOI process in combination with various radiation-hardened-by-design (RHBD) techniques to mitigate TID and single-event effects in standard cell designs.

Specialized library cells, such as SET filters, voters, and DICE-based sequential cells, are provided to support design methodologies capable of implementing system-level SEE immunity for LET levels over 60 MeV/cm^2.mg.

Physical Dimensions

DARE22G standard cells are based on a custom 10-track single-height standard cell layout template.

Parameter	Value
Cell height	0.8 µm
Cell column (poly pitch)	104 nm
Intra-cell metallization	M1, M2, C1
Supply rail layer	M1
Supply rail width	80 nm
Metal routing orientation	VHV
Lowest metal routing layer	M2
Routing pitch (M2)	80 nm
Routing offset (M2)	80 nm

Contact

For further information, please contact us at
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Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	Minimum	Typical	Maximum	Unit
Supply voltage	V_{DD}	0.72	0.8	0.88	V
Operating temperature	T_J	-40	25	125	°C
TID threshold	TID_{th}	100			krad (SiO_2)
LET threshold (SEL)	LET_{th_SEL}	70			MeV.cm^2/mg