DARE22G
I/O Library

Product Brief

Features

DARE22G I/O main features include:

- · Pad-limited fixed-height narrow layout
- I.8/3.3 V multi-domain enablement
- Distributed power-on control
- Programmable digital I/O cells
- Cold-spare functionality (1.8 V cells only)
- Horizontal and vertical placement supported
- Inline and staggered pad arrangement supported
- 2 kV ESD protection (HBM)
- TID immunity over 100 krad (SiO₂)
- SET immunity over 60 MeV.cm²/mg
- SEL immunity over 70 MeV.cm²/mg

Physical Dimensions

DARE22G I/O library employs a pad-limited fixed-height narrow layout construction with wide supply rails to support large pin counts and high output currents.

Parameter	Value
Pad arrangement	inline/staggered
Cell height	89 µm
Cell width	0.5 ~ 60 μm
Cell placement grid	0.5 µm

Contact

For further information, please contact us at dare@imec.be

Product Overview

DARE22G provides a comprehensive radiation-hardened I/O library for the implementation of 1.8 V and 3.3 V multi-domain mixed-signal I/O interfaces in the commercial GF 22 nm FDSOI CMOS process.

DARE22G exploits the intrinsic SEL immunity provided by the FDSOI technology in combination with special radiation-hardening-by-design (RHBD) techniques to mitigate TID and single-event effects in I/O rings.

I/O Library

DARE22G I/O library combines 1.8 V and 3.3 V domain cells. Special adapter breaker cells enable the integration of 1.8 V and 3.3 V interface domains in a single I/O ring.

Cold-Spare I.8 V I/O Cells

- Analog I/O cells
- Digital programmable I/O cells
- Back-gate biasing supply cells
- Power-on control cells
- Core and I/O supply cells
- Isolated core and I/O supply cells
- Full and partial domain breaker cells
- · Corner and filler cells

3.3 V I/O Cells

- Digital programmable I/O cells
- Power-on control cells
- Full domain breaker cells
- I.8 V domain adapter cells
- Corner and filler cells

Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	M inimum	Typical	M aximum	Unit
Core supply voltage	V_{DD0V8}	0.72	0.8	0.88	V
I/O supply voltage					
- 1.8 V I/O domain	V_{DDIV8}	1.62	1.8	1.98	V
- 3.3 V I/O domain	V_{DD3V3}	2.97	3.3	3.63	V
I/O voltage	$V_{I/O}$				
- I.8 V I/O domain		-0.3		1.98	V
- 3.3 V I/O domain		-0.3		3.63	V
Operating temperature	T_J	-40	25	125	°C
ESD rating (HBM)	V_{HBM}	2			kV
TID immunity	TID	100			krad (SiO ₂)
SET hardening	SET_th	60			MeV.cm ² /mg
SEL hardening	SEL_th	70			MeV.cm ² /mg