Product Overview

DARE22G provides a set of standard cell library variants for the implementation of radiation-hardened digital core circuits in the commercial GF 22 nm FDSOI CMOS process.

Each library variant implements the same cell set using a different combination of Vt flavor and gate length to provide distinct speed and leakage trade-offs that can be further adjusted via back-gate bias voltage tuning.

Vt Flavor	Gate Length	Well Structure
SLVT	20 nm	FBB (flip well)
SLVT	24 nm	FBB (flip well)
SLVT	28 nm	FBB (flip well)
LVT	20 nm	FBB (flip well)
LVT	24 nm	FBB (flip well)
LVT	28 nm	FBB (flip well)
RVT	20 nm	RBB (conventional well)
RVT	24 nm	RBB (conventional well)
RVT	28 nm	RBB (conventional well)
HVT	20 nm	RBB (conventional well)
HVT	24 nm	RBB (conventional well)
HVT	28 nm	RBB (conventional well)

All libraries are based on a common layout template which allows the combination of matching-well variants within the same standard cell design. As well, equivalent cells across different library variants implement same footprint which allows post-layout design optimizations via cell replacement without additional place & route iterations.

Library Cells

DARE22G standard cell libraries include the following categories of cells:

- Non-hardened combinational cells
- Non-hardened sequential cells
- SET-hardened combinational cells
- SEU-hardened sequential cells
- TMR enablement cells
- P&R enablement cells

Radiation Hardening

DARE22G exploits the intrinsic SEL immunity provided by the FDSOI technology in combination with special RHBD techniques to mitigate TID and single-event effects in standard cell designs.

SEE immunity can be achieved by employing a design methodology that is supported by the different types of cells available in the DARE22G core libraries. In this approach, regular standard cells are used in combinational data paths whereas cells rated at target LET thresholds up to 60 MeV/cm^2.mg are used for the implementation of clock trees and asynchronous circuitry. Flip-flops and latches based on the DICE architecture provide SEU-hardening in register elements rated at an LET threshold above 60 MeV/cm^2.mg. Special library cells are available to support SET filtering and TMR implementations.

Physical Dimensions

DARE22G core cells are implemented on a 10-track single-height standard cell layout template.

Parameter	Value
Cell height	0.8 µm
Cell column (poly pitch)	104 nm
Intra-cell metallization	M1, M2, C1
Supply rail layer	M1
Supply rail width	80 nm
Metal routing orientation	VHV
Lowest metal routing layer	M2
Horizontal routing pitch	80 nm
Horizontal routing offset	80 nm

Contact

For further information, please contact us at
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Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	Minimum	Typical	Maximum	Unit
Supply voltage	VDD	0.72	0.8	0.88	V
Operating temperature	T_J	-40	25	125	°C
TID immunity	TID	100			krad (SiO_2)
SEL hardening	SEL_{th}	70			MeV.cm^2/mg